

IN THE CLAIMS

We claim:

1. A method of forming a passivation layer on a semiconductor substrate, said method comprising the steps of:

forming a first dielectric layer over a metal interconnect layer on a substrate, said metal interconnect layer including a bond pad and a metal member spaced apart from said bond pad by a gap, said first dielectric formed over said bond pad and said metal member and in said gap; and

forming a second dielectric layer over said first dielectric layer, wherein said second dielectric layer is hermetic and has a larger dielectric constant than said first dielectric.

2. The method of claim 1 wherein said first dielectric layer is at least as thick as said metal layer.

3. The method of claim 1 wherein said first dielectric layer comprises silicon dioxide.

4. The method of claim 1 wherein said second dielectric layer comprises silicon nitride.

5. The method of claim 1 wherein said second dielectric layer is thinner than said first dielectric layer.

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6. A method of forming a hermetically sealed integrated circuit, said method comprising the steps of:

forming a first dielectric layer on a top surface of a bond pad on a substrate;

forming a second dielectric layer on said first dielectric;

forming an opening through said second dielectric and said first dielectric so as to expose said top surface of said bond pad;

depositing a conducting barrier layer on the sides of said opening and on said top surface of said bond pad; and

forming a bump on said barrier layer in said opening.

7. The method of claim 6 wherein said second dielectric layer and said barrier layer are resistant to moisture penetration.

8. The method of claim 7 wherein said first dielectric layer comprises silicon dioxide and said second dielectric layer comprises silicon nitride.

9. The method of claim 6 wherein said conductive barrier layer comprises a lower titanium layer and a top nickel-vanadium layer.

10. The method of claim 6 wherein said bump is formed by electroplating plating.

11. A method of forming a low interconnect capacitance wafer passivation, said method comprising the steps of:

forming a metal layer having a first member spaced from a second member by a gap;

forming a first dielectric layer over said first and second members and in said gap wherein said gap is completely filled by said first dielectric layer;

forming a second dielectric layer over said first dielectric layer, wherein second dielectric layer has a higher dielectric constant than said first dielectric;

forming an opening through said second dielectric and said first dielectric to expose the top surface of at least one of said spaced apart members;

forming a barrier metal on the sidewalls of said opening and over the top surface of said at least one spaced apart member; and

forming a contact on said barrier metal in said opening.

12. The method of claim 11 further comprising the steps of:

after forming said second dielectric and prior to forming said barrier layer, forming a third dielectric layer over said second dielectric layer.

13. The method of claim 11 wherein said contact is a bump.

14. The method of claim 13 wherein said bump is formed by electroplating plating.

15. The method of claim 11 wherein said first dielectric layer comprises silicon dioxide.

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16. The method of claim 11 wherein said first dielectric layer comprises silicon dioxide doped with fluorine.
 17. The method of claim 11 wherein said second dielectric layer comprises silicon nitride.
 18. The method of claim 12 wherein said third dielectric layer comprises a polyimide.
 19. The method of claim 11 wherein said first dielectric layer is thicker than said second dielectric layer.
20. The method of claim 11 wherein said barrier layer comprises a lower titanium layer and an upper nickel vanadium layer.
21. A passivation film formed over a substrate, said passivation film comprising:
a first dielectric layer formed over a metal interconnect layer formed on a substrate, said metal interconnect layer comprising a metal member spaced from a bond pad by a gap, said first dielectric layer formed over said bond pad and said metal member and completely filling said gap; and
a second dielectric layer formed over said first dielectric layer, said second dielectric layer having a dielectric constant greater than said first dielectric layer.

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22. The passivation structure of claim 21 wherein said first dielectric layer has a dielectric constant ≤ 4.0 .
23. The passivation structure of claim 22 wherein said first dielectric layer is silicon dioxide.
24. The passivation structure of claim 21 wherein said second dielectric layer is resistant to moisture penetration.
25. The passivation structure of claim 24 wherein said second dielectric layer is silicon nitride.
26. A passivation structure, said passivation structure comprising:
a first dielectric layer formed on a top surface of a bond pad on a substrate, said first dielectric layer having sidewalls on said bond pad;
a second dielectric layer on said first dielectric layer; and
an electrical contact formed through said first dielectric layer and said second dielectric layer and in contact with said bond pad, said electrical contact directly adjacent to and in direct contact with said sidewalls of said first dielectric layer.
27. The passivation structure of claim 26 wherein said second dielectric layer and said electrical contact are resistant to moisture penetration.

28. The passivation structure of claim 26 wherein said first dielectric layer comprises silicon dioxide and said second dielectric layer comprises silicon nitride.

29. The passivation structure of claim 26 wherein said electrical contact comprises a lower conductive barrier layer and a metal bump.

30. The passivation structure of claim 29 wherein said lower conductive barrier layer comprises a lower titanium layer and a top nickel vanadium layer.

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